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THE TUNED LOAD POWER AMPLIFIER

EL AMPLIFICADOR DE POTENCIA DE CARGA SINTONIZADA

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Abstract: This paper shows the design and simulation results of a hybrid tuned load power amplifier. The amplifier has been designed at 2.4 GHz, obtaining saturated drain efficiency above 70 %, together with a small signal gain of 15 dB. The deduction of design and analysis equations is presented considering class AB bias conditions and FET device assumption. A Cree's GaN-HEMT CGH40010F device has been used with a nonlinear model guarantied up to 6 GHz and with an expected output power of 10 W. The simulation has been carried out using Agilent ADS CAD tools.

Keywords: Power Amplifier, high efficiency, GaN devices, Tuned Load, Microwave Circuits.

Resumen: Este artículo muestra el diseño y los resultados de simulación de un amplificador de potencia de carga sintonizada. El amplificador fue diseñado a 2.4 GHz, obteniendo una eficiencia en saturación arriba del 70 %, junto con una ganancia a pequeña señal de 15 dB. La deducción de ecuaciones de diseño y análisis es presentada considerando condiciones de polarización clase AB y asumiendo el uso de dispositivos FET. Un dispositivo CGH40010F fabricado por Cree Corporation ha sido usado con un modelo no lineal válido hasta 6 GHz y una potencia de salida esperada de 10 W. La simulación se ha llevado a cabo usando la herramienta CAD ADS.

Palabras clave: Amplificador de potencia, alta eficiencia, dispositivos GaN, Carga Sintonizada, Circuitos de microondas.

1. INTRODUCTION

At the transmitter of a wireless communication system, before the antenna, a high frequency power amplifier is usually present. This amplifier has to increase the modulated signal's power to be transmitted by the antenna (Gagliardi, 1978). A simplified transmitter block scheme is shown in Fig. 1.

The three most important figures of merit for a power amplifier are gain, output power and efficiency. The latter is directly related to the DC power consumption, which means that, if a power amplifier is not efficient enough; more energy dissipation is produced through the device and passive structures of the circuit, increasing the transmission cost of the system. Also, detrimental effects will be experienced in addition to shorter device lifetime, cooling system inclusion and poor compactness, these latter due to the high heat dissipation (Moreno *et al.*, 2012).

Some methods to design high efficiency power amplifiers have been developed (Colantonio *et al.*, 2009), which include switched (Sokal and Sokal, 1975; El-Hamamsy, 1994) and harmonic tuned power amplifiers (Colantonio *et al.*, 2009; Raab, 1997).

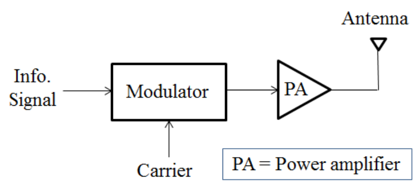

Fig. 1: Simplified block scheme of a transmitter in a wireless communication system.

In this paper, design and analysis equations are presented for the tuned load power amplifier, including class AB bias conditions and FET device assumption. This class of power amplifier belongs to the harmonic tuned set. It is not a big problem to notice that the design equations could be easily transformed to use them in other kind of devices.

Finally, for the sake of completeness, a design of a tuned load power amplifier at 2.4 GHz using a Cree's GaN-HEMT device and Taconic's RF35 substrate is carried out.

2. TUNED LOAD POWER AMPLIFIER

In terms of efficiency, gain and output power of a power amplifier, the performances are strictly related to the voltage and current waveforms at the device's intrinsic drain. Hence, the output matching network might be synthesized in order to generate the needed waveforms, for maximizing the mentioned figures of merit (efficiency, gain and/or output power) (Colantonio *et al.*, 2009; Cripps, 1999).

In fact, the efficiency depends on the DC power consumption and on the RF power delivered to the fundamental frequency. As expected, some part of the DC power consumption is dissipated as RF power at the fundamental frequency, while the other part is dissipated at the device and at the drain harmonic terminations. Therefore, if overlapping between intrinsic drain voltage and current waveforms is avoided, and no power is delivered to the harmonic terminations, the efficiency will reach 100 %, at least in principle (Moreno, 2012).

The Tuned Load Power Amplifier exploits those conditions. In order to avoid power dissipation at the harmonics terminations, the idea is zeroing their impedance (short-circuit terminations). At the fundamental frequency, the load is totally real and should exploit the device's power capabilities. In addition, it is not difficult to notice that with this kind of loads, the Tuned Load Power Amplifier avoids (up to certain point) the overlapping between the drain current and voltage waveforms.

The general scheme for a power amplifier with the conditions for the Tuned Load stage is shown in Fig. 2. Considering a FET device biased in class AB and sinusoidal driving, the dynamic load curve at the intrinsic drain with Tuned Load conditions, should be as shown in Fig. 3 for its maximum swing before saturation.

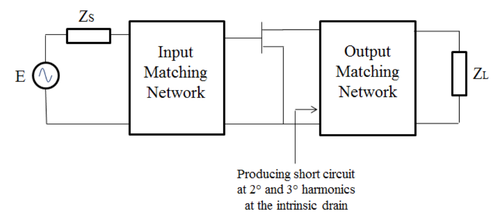

Fig. 2: Tuned Load Power Amplifier general scheme.

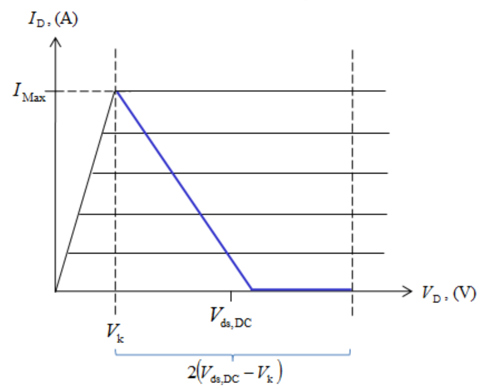

Fig. 3: Tuned Load Power Amplifier dynamic load curve.

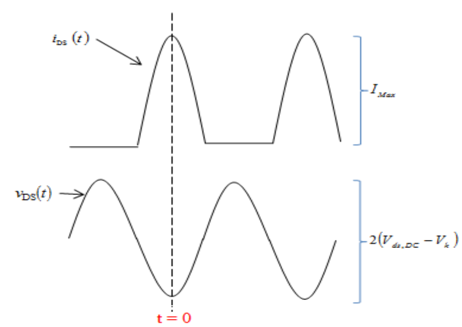

Fig. 4: Drain current and voltage waveforms for a Tuned Load Power Amplifier.

Given by the class AB bias conditions and sinusoidal gate driving, the drain current waveform is expected to be a truncated sinusoidal, as presented in Fig. 4. On the other hand, the short-circuit terminations for the harmonics and real for the fundamental frequency, synthesize a pure sinusoidal drain voltage (Fig. 4).

Therefore, the load at the fundamental frequency can be calculated as:

$$R_{TL} = \frac{V_{ds,DC} - V_k}{I_1(f)} \qquad (1)$$

Where $V_{ds,DC}$ is the drain bias voltage, V_k is the device knee voltage and $I_1(f)$ is the fundamental component of the truncated sinusoidal drain current at its maximum swing with a conduction angle of f, and it is given by:

$$I_1(f) = \frac{I_{Max}}{2p} \frac{f - \sin f}{1 - \cos\left(\frac{f}{2}\right)} \qquad (2)$$

At the same time, the output power can be calculated as:

$$P_{out} = \frac{1}{2}(V_{ds,DC} - V_k) I_1(f) = \frac{I_{Max}}{4p}(V_{ds,DC} - V_k) \frac{f - \sin f}{1 - \cos\left(\frac{f}{2}\right)} \qquad (3)$$

And the drain efficiency is given by:

$$h_{TL} = \frac{I_{Max}(V_{ds,DC} - V_k)}{4pV_{ds,DC} I_0(f)} \frac{f - \sin f}{1 - \cos\left(\frac{f}{2}\right)} \qquad (4)$$

Where $I_0(f)$ is the DC component of the truncated drain current, it is:

$$I_0(f) = \frac{I_{Max}}{2p} \frac{2\sin\left(\frac{f}{2}\right) - f\cos\left(\frac{f}{2}\right)}{1 - \cos\left(\frac{f}{2}\right)} \qquad (5)$$

As an example, considering an idealized device biased in class B ($f = p$), with $V_k = 0$, the efficiency in saturation will be p/4 = 78.5%. For the sake of comparison, for an amplifier in class A bias conditions, the efficiency will be only 50%.

3. A 65% EFFICIENCY 13 WATTS POWER AMPLIFIER AT 2.4 GHz

The realized power amplifier is based on the CGH40010 GaN-HEMT (Shealy *et al.*, 2002; Binari *et al.*, 1997) fabricated by Cree Corporation (CGH40010 Datasheet; 2011), a package device capable of 10 W output power at 28 V drain bias and operative frequency range 0-6 GHz.

Using cold-FET simulations (Lu, 2008), an accurate model of the parasitics have been obtained, allowing the identification of the load for the externally accessible terminals (extrinsic drain) that generates the right load at the intrinsic ones (Park, 2006).

The IV-curves that characterize the GaN-HEMT device are shown in Fig. 5. It can be noticed that a knee voltage around 3 volts could be considered. Considering $I_{Max} = 1.5$ A, and a conduction angle $f = 190^o$ ($I_{DS} = 0.1 I_{Max}$) for good linearity, the fundamental load is calculated using Equation (1):

$$R_{TL} = \frac{V_{ds,DC} - V_k}{I_1(f)} \approx 30\,\Omega \qquad (6)$$

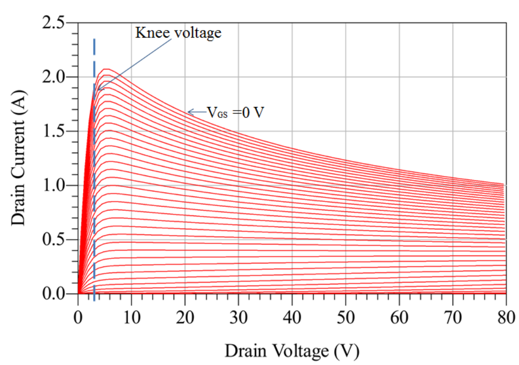

Fig. 5: IV characteristics of the selected device.

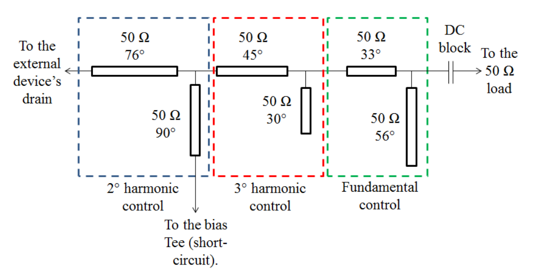

Fig. 6: Output matching network configuration. Electrical length of transmission lines refers to the fundamental frequency 2.4 GHz.

Thus, the designed output matching network is presented in Fig. 6. The first block at the left has to synthesize short-circuit at the intrinsic drain for the second harmonic, the second one does the same for the third harmonic and the block at the right tunes the load at the fundamental frequency.

The synthesized input matching network is shown in Fig. 7. In this case, additional circuitry has been added (*RC network*) in order to guarantee a Rollet's stability factor greater than unity, which means unconditional stability, avoiding in this way, possible oscillations (Pozar, 1999). The single stub transmission line network has been designed to produce input conjugate matching.

A bias Tee that operates as short-circuit at the fundamental frequency and harmonics has been used (see Fig. 8).

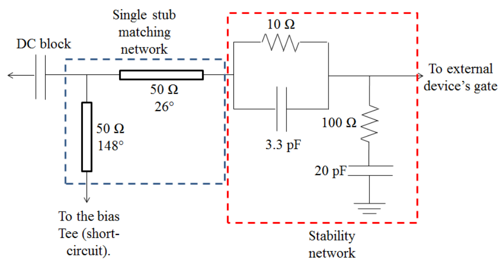

Fig. 7: Input matching network configuration. Electrical length of transmission lines refers to the fundamental frequency 2.4 GHz.

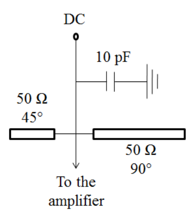

Fig. 8: Bias Tee configuration. Electrical length of transmission lines refers to the fundamental frequency 2.4 GHz.

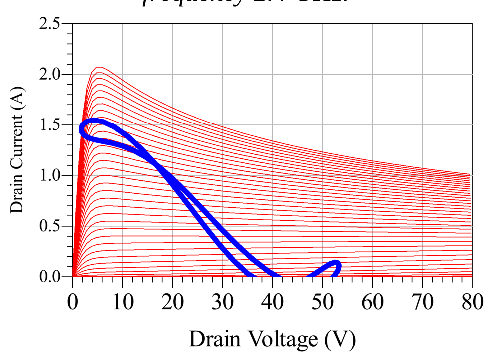

Fig. 9. Simulated dynamic load curve (blue) and IV-characteristics (red).

The simulated dynamic load curve is in good agreement with the expected for Tuned Load conditions (see Fig. 3) and it is shown in Fig. 9. Also, it is important to check the simulated drain current and voltage waveforms, which are shown in Fig. 10, both of them have been simulated at the beginning of saturation (notice that the dynamic load curve reaches the knee voltage).

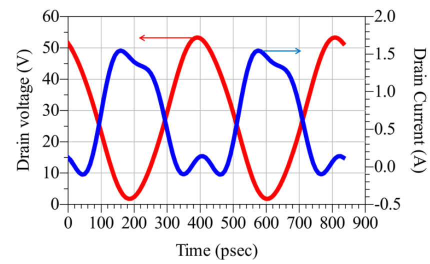

Fig. 10: Intrinsic drain current (blue) and voltage (red).

Output power, efficiency, transducer and operation gains versus input power are shown in Fig. 11. A 15 dB small signal gain has been obtained, together with maximum efficiency (in saturation) of 75 % and maximum output power of 41.5 dBm.

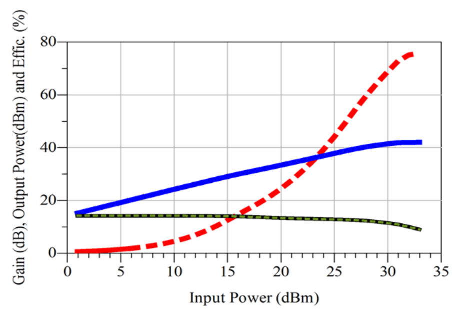

Fig. 11: Gain (green), output power (blue) and efficiency (red).

4. ACKNOWLEDGMENTS

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5. CONCLUSION

A Tuned Load hybrid high efficiency and high frequency power amplifier has been designed, obtaining 75% of maximum efficiency and 41.5 dBm of output power at 2.4 GHz. These performances place the present amplifier in possible applications for systems operating in the 2.4 GHz band.

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